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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,847	08/31/2001	Masayuki Sasaki	2001_1150A	8526

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WENDEROTH, LIND & PONACK, L.L.P.
2033 K STREET N. W.
SUITE 800
WASHINGTON, DC 20006-1021

EXAMINER

NGUYEN, SON XUAN

ART UNIT PAPER NUMBER

2664

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/942,847

Applicant(s)

SASAKI, MASAYUKI

Examiner

SON X. NGUYEN

Art Unit

2664

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 August 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☒ Claim(s) 13 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 August 2001 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2/9/05</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 9-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 9, the limitation recited in lines 2 of page 71 "empty one" is unclear and confusing. Examiner could not understand of what being claimed.

Claims 10-12 are rejected based on rejected independent claim 9.

Claim Rejections - 35 USC § 103

3. Claims 1,2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rouphael et al. (U.S 6,801,564) in view of Philips (U.S 6,307,877).

Regarding claim 1, Rouphael discloses a CDMA base transceiver system **(Reverse Link Correlation Filter in Fig. 1)**, the CDMA base transceiver system adapted to perform wireless communications through the use of a CDMA method, comprising: an FPGA that processes a signal at a chip rate through the use of FPGA program data **(FPGA receives and processes input signal at chip rate; See FPGA 5**

Art Unit: 2664

in Fig. 3); a DSP that processes a signal at a symbol rate through the use of DSP program data (DSP receives and processes input signal at symbol rate; See lines 32-36 of column 2 and DSP 4 in Fig. 3);

Rouphael, however, fails to disclose program data setting means that sets the FPGA program data used by the FPGA and the DSP program data used by the DSP.

Philips teaches program data setting means that sets the FPGA program data used by the FPGA and the DSP program data used by the DSP (Computer 506 of Fig. 7 is external programming device which provides programming for FPGA and DSP; See lines 2-5 of column 10).

It would have been obvious to one ordinary skill in the art at the time the Invention was made to combine a computer with FPGA and DSP for the purpose of enabling to program the FPGA and DSP with external computer, the motivation of programming FPGA and DSP would be capable of customizing settings for FPGA and DSP to meet specific needs.

Regarding claim 2, Rouphael discloses a CDMA base transceiver system (Reverse Link Correlation Filter in Fig. 1).

Rouphael, however, fails to disclose memory connection means through the use of that there is connected to an external memory, whereby the program data setting means sets the program data by reading the program data stored in the external memory connected through the use of the memory connection means.

Philips teaches memory connection means (Serial port 538 of Fig. 7) through the use of that there is connected to an external memory (EPROM 534a of Fig. 8; See

lines 67 of column 7 and lines 1-2 of column 8), whereby the program data setting means (Computer 506 of Fig. 7 is external programming device which provides programming for FPGA and DSP; See lines 2-5 of column 10) sets the program data by reading the program data stored in the external memory connected through the use of the memory connection means.

It would have been obvious to one ordinary skill in the art at the time the invention was made to combine a serial port and external memory EPROM for the purpose of enabling to store software data for FPGA and DSP and to provide access to these data, the motivation of using serial port and external memory EPROM would be capable of programming all settings for FPGA and DSP.

Regarding claims 3 and 4, Rouphael discloses a CDMA base transceiver system (Reverse Link Correlation Filter in Gig. 1).

Rouphael, however, fails to disclose program data setting means sets the program data corresponding to a type of communication method that is selected from among a plurality of communication methods that includes two or more types of communication methods of a W-CDMA/TDD method, a W-CDMA/FDD method, and a multi-carrier CDMA method; and the FPGA and DSP each processes a signal through the use of said communication method.

Philips teaches program data setting means (Computer 506 of Fig. 7 is external programming device which provides programming for FPGA and DSP; See lines 2-5 of column 10) sets the program data corresponding to a type of communication method that is selected from among a plurality of communication

Art Unit: 2664

methods that includes two or more types of communication methods of a W-CDMA/TDD method, a W-CDMA/FDD method, and a multi-carrier CDMA method; and the FPGA and DSP each processes a signal through the use of said communication method **(The evaluation board 502 supports full flexibility in data rates, spreading techniques which implies all types of CDMA methods; See lines 32-35 of column 23).**

It would have been obvious to one ordinary skill in the art at the time the invention was made to combine external computer with software program data for the purpose of enabling to support plurality types of communication methods including W-CDMA/TDD method, a W-CDMA/FDD method, and a multi-carrier CDMA method, the motivation of using software program data supporting plurality types of communication methods would be capable of allowing Reverse Link Correlation Filter functions in different communication environments.

Regarding claims 5 and 8, Rouphael discloses a CDMA base transceiver system **(Reverse Link Correlation Filter in Fig. 1; See lines 21-25 of column 2)**, the CDMA base transceiver system adapted to perform wireless communications through the use of a CDMA method, comprising: a base band part **(Receiver 20 of Fig. 1)** that is constructed using an FPGA that processes a signal through the use of FPGA program data and a DSP that processes a signal through the use of DSP program data **(FPGA 5 and DSP 4 of Fig. 1; See lines 43-46 of column 3).**

Rouphael, however, fails to disclose program data changing means that changes the FPGA program data used by the FPGA and the DSP program data used by the DSP to program data corresponding to a different type of communication method.

Philips teaches program data changing means that changes the FPGA program data used by the FPGA and the DSP program data used by the DSP to program data corresponding to a different type of communication method **(Computer 506 of Fig. 7 is external programming device which provides programming for FPGA and DSP; See lines 2-5 of column 10)**

It would have been obvious to one ordinary skill in the art at the time the Invention was made to combine a computer with FPGA and DSP for the purpose of enabling to program the FPGA and DSP with external computer, the motivation of programming FPGA and DSP would be capable of customizing settings for FPGA and DSP to meet specific needs.

Regarding claim 6, Roupahel discloses a CDMA base transceiver system **(Reverse Link Correlation Filter in Fig. 1);**

Roupahel, however, fails to disclose clock that supplies a chip-rate clock having a frequency corresponding to the chip rate of each of a plurality of the communication methods changeable by the program data changing means and that supplies a symbol-rate clock having a frequency corresponding to the symbol rate of each of a plurality of the communication.

Philips teaches clock means **(Clock generator 302 of Fig. 3; See lines 59-64 of column 9)** that supplies a chip-rate clock having a frequency corresponding to the chip rate of each of a plurality of the communication methods changeable by the program data changing means and that supplies a symbol-rate clock having a frequency corresponding to the symbol rate of each of a plurality of the communication methods

Art Unit: 2664

(Programmable frequency is programmed to support all data rates; See lines 51-54 of column 19).

It would have been obvious to one ordinary skill in the art at the time the invention was made to combine a clock generator with Reverse Link Correlation Filter for the purpose of providing frequency at different rates, the motivation of providing frequency at different rates would be capable of allowing Reverse Link Correlation Filter process data at different data rates.

Regarding claim 7, Roupahel discloses a CDMA base transceiver system **(Reverse Link Correlation Filter in Gig. 1);**

Roupahel, however, fails to disclose the clock means oscillates a clock signal having a frequency that has the value of a common multiple of the frequency corresponding to the chip rate of the W-CDMA method and the frequency corresponding to the chip rate of the multi-carrier CDMA method, thereby supplying a chip-rate clock and a symbol-rate clock.

Philips teaches clock means **(Clock generator has at least one numerically controlled oscillator; See lines 59-63 of column 5)** oscillates a clock signal having a frequency that has the value of a common multiple of the frequency corresponding to the chip rate of the W-CDMA method and the frequency corresponding to the chip rate of the multi-carrier CDMA method, thereby supplying a chip-rate clock and a symbol-rate clock **(Frequency is programmed or set to supply a chip-rate clock and a symbol-rate clock; See lines 30-55 of column 29).**

It would have been obvious to one ordinary skill in the art at the time the

Art Unit: 2664

invention was made to combine a clock generator with Reverse Link Correlation Filter for the purpose of providing frequency having different value, the motivation of providing frequency at different value would be capable of allowing Reverse Link Correlation Filter providing timing signal at different frequency rates corresponding to different communication method.

Allowable Subject Matter

4. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a) Philips et al. (U.S 6,307,877) Programmable modem apparatus for transmitting and receiving digital data, design method and use method for said modem.
- b) Rouphael et al. (U.S 6,801,564) Reverse link correlation filter in wireless communication systems.
- c) Lugil et al. (US 2002/0196754) Method and system for high-speed software reconfigurable code division multiple access communication.

Art Unit: 2664

d) Andersson et al. (U.S 6,400,966) Base station architecture for a mobile communications system.

e) John Walley (U.S 5,778,022) Extended time tracking and peak energy in-window demodulation for use in a direct sequence spread spectrum system.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SON X. NGUYEN whose telephone number is 571-272-6048. The examiner can normally be reached on 8 AM -5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Son Xuan Nguyen 4/11/05



KENNETH VANDERPUYE
PRIMARY EXAMINER